UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/604,567 | 07/30/2003 | Gong-Sheng Lin | MTKP0085USA | 1566 |

27765 7590 01/04/2007

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

| EXAMINER | |
|---|---|
| HUNG, YUBIN | |
| **ART UNIT** | **PAPER NUMBER** |
| 2624 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 01/04/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/604,567 | LIN ET AL. | |
| | Examiner | Art Unit | |
| | Yubin Hung | 2624 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-17* is/are allowed.

6)☒ Claim(s) *1, 3, 5-7 and 9* is/are rejected.

7)☒ Claim(s) *2,4 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to because:

- Fig. 6: "<=" is used to indicate assignment of value; however, "<=" can easily be interpreted as "less than or equal to" and therefore is misleading; consider using "←" or ":=" instead

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Specification***

2. The disclosure is objected to because of the following informalities:

- Adjacent words run into each other in numerous places, e.g., paragraph 9, line 12 ("formsa"), line 14 ("thespatially" and "avariable"), line 17 ("toconvert"); claim 10, line 1 ("ina")
- Claim 9, line 8: Per Fig. 4, refs. 410 & 412 and the last four lines of paragraph 41, "A0" should have been "A1" **[Note: per communication with Applicant's representative Mr. Scott Margo on 12/14/06, for examination purpose claim 9 will be interpreted with A0 changed to A1.]**

Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**4. Note: Since the definitions of A0-A3, D0, X0, X1, Y0 and Y1 are not given in the claims, for examination purpose Fig. 1 and paragraph 10 of the instance application will be relied upon to interpret claims 1-17 for their meanings.**

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,563,953), and further in view of Hayashi (US 5,717,462).

6. Regarding claim 1, Lin discloses an apparatus [Fig. 9; Col. 13, lines 6-7] for calculating prediction bits for a spatially predicted coded block pattern [Figs. 6-8; Col. 11, line 44-Col. 12, line 16; note that Y1-Y4 in the 2x2 block (ref. 126) of Fig. 6 correspond to A0-A3, respectively, and the five immediate neighbors of block 126 (one Y2, one Y3 and three Y4) correspond to D0, X0, X1, Y0 and Y1 (in the manner as shown in Fig. 1 of the instance application, e.g., Y3 corresponds to X0)].

Lin further discloses

- a storage device storing rows of bits including the spatially predicted coded block pattern, a DO bit, an X0 bit, an Xl bit, a Y0 bit, and a Y1 bit
  [Per the discussion above, Figs. 6-8 & Col. 11, line 44-Col. 12, line 6 disclose setting bits A0-A3 using D0, X0, X1, Y0 and Y1. While the storing of the bits is not expressly disclosed, since this operation is implemented using the system of Fig. 9 (see Col. 13, lines 6-7), the required row bits necessarily have to be stored in a storage device such as ref. 922 (system memory)]
- a circuit connected to the storage device for setting the A0 bit and for setting the A2 bit
  [Fig. 9, ref. 921 (processing unit, a kind of circuit, which is connected to storage device 922). Note that clearly the instructions carrying the bit setting operation are executed by the processing unit. Note further that while Figs. 6-8 & Col. 11, line 44-Col. 12, line 6 only expressly discloses how to set bit A0 (shown as Y1 in Fig. 6), it

is clear that bits A1-A3 are set in like manner (see also Col. 10, lines 19-31), but not necessarily in sequence]

Lin does not expressly disclose that two separate circuits connecting to the same storage device are used to set the values of A0 and A2 in parallel.

However, Hayashi teaches using multiple circuits when parallel processing is desired (e.g. to set multiple prediction values in parallel). [Fig. 2, refs. 30-1 through 30-5 (parallel prediction processors, each a kind of circuit) and Col. 18, lines 59-60. Note that the processors are connected to ref. 11, a storage device.]

Lin and Hayashi are combinable because they both have aspects that are from the same field of endeavor of compression.

At the time of the invention it would have been obvious to one of ordinary skill in the art to modify Lin with the teachings of Hayashi by using separate circuits to compute A0 and A2 in parallel. The motivation would have been to improve processing speed [such benefit is indicated in column 6, lines 15-17 and 31-33 (using parallel block matching means, each a circuit, shown as refs. 161-163 in Fig. 4) of Hayashi].

Therefore it would have been obvious to combine Hayashi with Lin to obtain the invention as specified in claim 1.

*****

7. Claims 3, 5-7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,563,953) and Hayashi (US 5,717,462) as applied to claim 1 above, and further in view of Ericsson (US 5,001,560).

8. Regarding claim 3, the combined invention of Lin and Hayashi discloses all limitations of its parent, claim 1. Lin also discloses comparing bits D0 and X0 (i.e., indicating whether they are equivalent) [Fig. 6, refs. 136a (Y4, considered as D0) & 134a (Y3, considered as X0); Fig. 7, ref. 142; Col. 11, line 67-Col. 12, line 2] and selectively setting A0 (shown as ref. 130a) to X0 (shown as ref. 134a) or Y0 (shown as ref. 132a), depending on the comparison result [Fig. 6, 130a (considered A0); Figs. 7 & 8 and Col. 12, lines 5-16. Note that depending on the value of Fig. 7, ref. 140 (i.e., the XOR result, which shows whether the two values are equivalent, i.e., both are 0 or both are 1; see also col. 12, lines 5-6), along with other conditions, the value of A0 (Fig. 6, ref. 130a) is set to either X0 (Fig. 6, ref. 134a) or Y0 (Fig. 6, ref. 132a)]. Note further that as discussed in the analysis of claim 1, the above comparison/value setting operations are executed in a processor (which is a kind of circuit) [Fig. 9, ref. 921; Col. 13, lines 8-9].

The combined invention of Lin and Hayashi does not expressly disclose that the circuit comprises a comparator (for carrying out the comparison to indicate equivalence) and a multiplexer (for setting values) that are both connected to a storage device.

However, Ericsson discloses a circuit comprising a comparator [Fig. 12 (corresponding to ref. 49 of Fig. 4), ref. 406; Col. 12, line 52-Col. 13, line 27] and a multiplexer [Fig. 12, ref. 410] that are both connected to a storage device [Fig. 4, refs. 44 (storage); see also ref. 56 of both Figs. 4 & 12]. Note further that the comparator compares two inputs and the multiplexer selects one of its own two inputs based on the output of the comparator; therefore they are capable of performing the functions of the first comparator and the first multiplexer as recited in the claim.

The combined invention of Lin and Hayashi is combinable with Ericsson because they both have aspects that are from the same field of endeavor of compression.

At the time of the invention it would have been obvious to one of ordinary skill in the art to modify the combined invention of Lin and Hayashi with the teachings of Ericsson by using the circuit recited above to carry out the comparison and the value setting operations. The motivation would have been to facilitate real-time processing, as Ericsson indicates in column 2, lines 40-41.

Therefore it would have been obvious to combine Ericsson with Lin and Hayashi to obtain the invention as specified in claim 3.

9. Claim 5 concerns using the same type of circuit recited in claim 3 (comprising a comparator and a multiplexer) for setting the value of A2 (corresponding to Y3 of the

2x2 block indicated by Lin's Fig. 6, ref. 126) basing on whether A0 (corresponding to Y1 of ref. 126) and Y0 (corresponding to Fig. 6, ref. 132a) are equivalent. Since, as per the analysis for claim 1 above, Lin discloses setting bits A1-A3 in the same manner as it does A0, the same analysis for claim 3 above applies to claim 5 and therefore claim 5 is similarly rejected.

10. Regarding claim 6, note that Hayashi further discloses a 3rd and a 4th circuits [Fig. 2, refs. 30-3 and 30-4] parallel to the 1st and the 2nd circuits [Fig. 2, refs. 30-1 and 30-2] for setting prediction values in parallel and the motivation for using these two additional circuits would have been to further improve the processing speed since there are four bits (A0-A1) to be set.

11. Claim 7 and claim 9 as interpreted are similarly analyzed and rejected as per the analyses of claims 5 and 6 above, respectively.

***Allowable Subject Matter***

12. Claims 10-17 are allowed.

13. Claims 2, 4 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter:

A. Regarding claim 2, closest art of record Lin et al. (US 6,563,953) and Hayashi (US 5,717,462) in combination discloses an apparatus as recited in claim 1. De Bergh (US 4,496,916) et al. further discloses a circuit that comprises a shift register [Fig. 2, ref. 23], in addition to a comparator and a multiplexer. However, none of the references cited above, alone or in combination, disclose, teach or suggest using the shift register in the manner recited in claim 2.

B. Regarding claim 4, and similarly claim 8, closest art of record Lin et al. (US 6,563,953), Hayashi (US 5,717,462) and Ericsson (US 5,001,560) in combination discloses an apparatus as recited in claim 3. Zydek et al. (US 6,012,156) et al. further discloses a circuit that comprises a NOR-gate [Fig. 2, ref. 30], in addition to a comparator and a multiplexer. However, none of the references cited above, alone or in combination, disclose, teach or suggest using a NOR-gate in the manner as recited in claim 4.

C. Regarding claim 10, closest art of record Lin et al. (US 6,563,953) and Hayashi (US 5,717,462) discloses a method that set prediction bits, including setting A0 and A2, in parallel. APA (admitted prior art: Fig. 1, and paragraphs 10-16 of the instance

application) further discloses, when X0 is equivalent to D0, setting A0 to Y0 [Paragraph 12] but A2 to Y1 only if A0 is also equivalent to Y0 [paragraph 14]. However, none of the references cited above, alone or in combination, disclose, teach or suggest setting A2 to Y1 as long as X0 is equivalent to D0, as required by claim 10.

***Conclusion and Contact Information***

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Holmes et al. (US 2005/0254605) – discloses parallel computing of a coded block pattern [Paragraphs 60-66 on pages 5 and 6]

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yubin Hung whose telephone number is (571) 272-7451. The examiner can normally be reached on 7:30 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jingge Wu can be reached on (571) 272-7429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Yubin Hung
Patent Examiner
Art Unit 2624

December 21, 2006

12/26/06